CPT-R09 Card

Red Phase Instruments TMS320F2810 DSP Controller Card

Technical Brief

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Card Version 1.2

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CPT-R09 Manual Revision History

CARD VERSION 1.0: Initial Board for prototype purposes.

No Manual Released

CARD VERSION 1.1: Rework for production

Release 1.0 – Initial Release of Manual.

CARD VERSION 1.2: Rework with larger labels for connectors,
4 pin power connector
USB cable reversed

Release 1.1 –Manual Revised for above changes

Table of Contents

CPT-R09 DSP Based Inverter Controller

1.0 Overview of the CPT-R09

The CPT-R09 is a low cost, high performance DSP based inverter controller that has been designed to act as a central, high-speed, flexible controller for a new range of Red Phase Instruments products.

The board is based around a Texas Instruments TMS320F2810PBK DSP, which has been specifically developed for use in digital motor/motion control applications, and contains on-card all necessary functions for a complete standalone inverter control system.

The CPT-R09 card measures 150mm x 115mm.

On-card facilities include:

- TMS320F2810PBK DSP processor
- 64k x 16 Flash (128k x 16 Flash on TMS320F2811PBK)
- 1k x 16 OTP ROM
- 4k x 16 Boot ROM
  - Software Boot Tables
  - Standard Math Tables
- 18K x 16 Single Access RAM (SARAM) made up of:
  - L0 and L1: 2 Blocks of 4K x 16 Each SARAM
  - H0: 1 Block of 8K x 16 SARAM
  - M0 and M1: 2 Blocks of 1K x 16 Each SARAM
- Serial Flash Memory with 1Mbit of non-volatile storage
- 1 off Power LED
- 4 off indication LEDs
- 4 off DIP switches
- 8 off open-collector digital outputs
- 2 off interrupt driven TTL-level digital inputs
- 8 off TTL-level individually configurable digital I/O bits
- 1 off SPI expansion interface, including chip selects
- 4 off precision reference ADC inputs (for calibration purposes)
- 12 off 12-bit 0-3V ADC inputs, with glitch filter and clamp diode protection
- 16 off complementary TTL-level gate driver PWM outputs, with common fault interrupt and enable
- Reset/Power-On Circuitry
- Power supply to generate all on-card supplies
- Power supply operation from input +12VDC

The card also supports the following peripheral interfaces:

- JTAG interface
- 1 off clocked Serial Peripheral Interface (also enables external Flash reprogramming)
- 1 off 3.3V-TTL serial interface
- 1 off isolated serial to USB interface

Figure 1-1 shows a functional block diagram of the CPT-R09 card, illustrating all major sections.

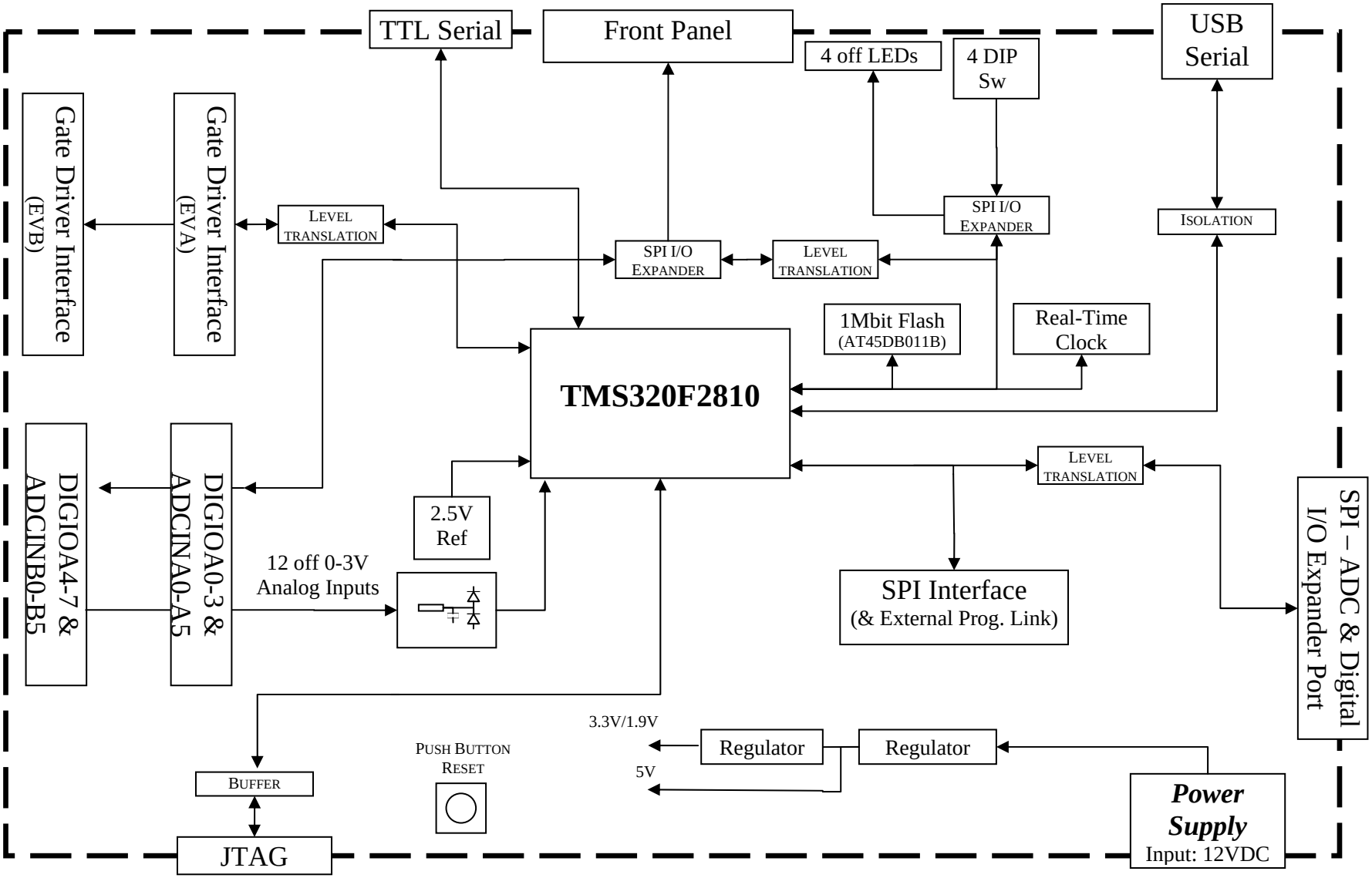

Figure 1-1: Functional Diagram of CPT-R09 DSP Controller Board

1.1 Digital I/O

The CPT-R09 card supports up to 42 bits of digital I/O, consisting of 8 bits for local I/O, 8 bits of buffered open collector outputs, 2 interrupt driven digital inputs and 24 bits of buffered TTL level I/O.

The local I/O consists of 4 bits driving LEDs mounted on-card and 4 bits of DIP switch inputs.

The 8 off buffered open collector outputs are able to drive off-card relays or LEDs from a +5V or +12V supply. The 2 off interrupt driven digital inputs are TTL-level, zener clamped inputs that are level shifted to 3.3V-TTL before feeding into INT1 and INT2 on the DSP chip.

The CPT-R09 card supports a maximum of 24 bits buffered digital I/O that can be configured as two banks of 8 digital outputs (shared with the Event Manager A and B PWM pins) and 2 banks of individually configurable 4-bit SPI driven expansion ports. All of these bits are provided buffered with a level translation from the 3.3V-TTL of the DSP to a TTL level output.

The CPT-R09 card can support an off card SPI to Digital I/O expansion bus, which enables interfacing to over 100 individually configurable digital I/O bits.

All 3.3V-TTL digital I/O pins on the TMS320F2810 chip have the capability to operate in either “Digital I/O or “Peripheral I/O” mode. The header files for the CPT-R09 board select the default modes of operation for all of the pins on the board. The user is advised to refer to this file before programming their software code.

1.2 Analog Inputs

The TMS320F2810 DSP has 16 off ADC inputs that accept voltages in the range of 0-3V. The analog inputs are divided into two banks of 8 (ADCINA0-7 and ADCINB0-7). Each bank feeds into an 8 to 1 analog multiplexer with a sample and hold circuit. The outputs from the two sample and hold circuits are fed directly into a single 12-bit ADC Module. The ADC module is capable of interleaving ADC conversions between the two banks to achieve a “pipelined” conversion process. This reduces the overall time required for “simultaneous” conversions. The maximum total conversion time for each ADC unit is 80ns (with a 25MHz ADC clock).

The CPT-R09 analog inputs are configured to provide 4 off precision reference inputs for self calibration and 12 off filtered external inputs to the TMS320F2810.

The CPT-R09 card has on-card precision 2.5V and 1.25V references that should be used for calibration of the internal ADC. Each ADC bank has a 1.25V and 2.5V reference fed to channels 6 and 7 for calibration purposes. It is strongly recommended that the ADC be software calibrated for both gain and offset. Please consult the Texas Instruments documentation on the ADC converter for further information. *TMS320x281x DSP Analog-to-Digital Converter (ADC) Reference Guide*, Literature Number: *SPRU060D*.

The 12 off filtered analog inputs are separated into A and B channels that are available on separate 20-way IDC headers. Each input has a low pass or “glitch” filter and a diode clamp circuit before they are fed into the DSP. The board accepts 0-3V inputs for these circuits.

A 2.5V reference is also available on each of the 20-way header for use off-card. It is recommended that this reference be fed into an off-card op-amp circuit for external buffering rather than being used directly.

1.3 Gate Drive Interface

The TMS320F2810 DSP supports 16 PWM channel outputs, made up of 6 complementary pairs (12 outputs) with programmable deadbands and 4 independent outputs generated by simple compare functions. The DSP chip has two independent event manager modules (EVA and EVB) and the PWM channels are evenly split between them. Dead band compensation must be software-calculated for the simple compare outputs.

The CPT-R09 is configured with two off 26-way headers, each of which contains 8 PWM channel outputs from a single Event Manager, in conjunction with a gate fault signal that is fed to the corresponding Event Manager PDPINT* interrupt pin. This enables a DSP hardware interrupt trip to immediately occur on detection of a fault,

thus disabling the PWM signals within 12 nanoseconds using hardware logic internal to the DSP. The card has pull-down resistors on the PWM outputs to ensure that they are left in a normally low state if a PDPINT* fault signal is triggered. A gate reset signal is also provided on each header to enable the off-card gate drivers to be reset in the event of a fault.

1.4 Communications

The CPT-R09 controller board supports three communication protocols: one off non-isolated 3.3V-TTL serial communications interface (SCI), a 3.3V-TTL synchronous serial peripheral interface (SPI) and an isolated USB serial communications interface.

The high-speed synchronous serial peripheral interface can be used to communicate to other computer systems. The interface can support either master or slave protocol, selected by software. The CPT-R09 has been provided with an SPI interface directly capable of reading from off-card SPI peripherals via the CPT-R08 26-way IDC header.

The isolated USB port uses an integrated USB UART IC to provide full PC handshaking that allows the port to appear like a conventional serial port. A driver must be installed onto the PC before the interface can operate correctly.

The 3.3V-TTL serial port can be used to communicate to a terminal emulation program, via an interface board, to aid in program development.

1.5 On-card memory

The CPT-R09 controller board supports 64k x 16bit of on-card Flash (128k x 16bit with the TMS320F2811), 18k x 16bit of SARAM and a 4k x 16 Boot ROM. Programs can be directly executed from RAM, via the JTAG interface or from Flash. By default, the card runs programs from the flash memory. Links are provided to enable RAM, SCI or SPI program operation.

In addition to the on-chip memory the CPT-R09 has a 1Mbit SPI interfaced Flash Memory chip for external data storage.

1.6 Power Supply

The standard CPT-R09 controller board operates from a nominal +12VDC. The board has on-card regulators that generate regulated +5V, +3.3V and +1.9V. These supplies are not isolated from the incoming +12V.

The USB interface is externally powered via the USB connector.

1.7 JTAG/programming

The CPT-R09 controller board has a JTAG interface for programming the DSP's Flash ROM or RAM. This port can also be used for emulator/debugging purposes using the Code Composer Studio Pod.

2.0 Specifications

2.1 Controller DSP Section

Processor	Texas Instruments TMS320F2810 (optional TMS320F2811)
On-card Memory	64k x 16 Flash Memory (128k x 16 TMS320F2811) 18k x 16 RAM 4k x 16 Boot ROM 1k x 16 OTP ROM
Reset	120ms hardware reset generated on-card from power up and supply failure. Can also be triggered via an on-card push button (**S2**)
Non-Volatile Memory Storage	1Mbit of memory storage using an SPI flash ROM chip Accessed via SPI interface on DSP
Interrupts	3 off masked external interrupts (XINT1, XINT2, XINT13/NMI) Support for 2 off PDPINT interrupts (on **X5** and **X6**)

2.2 Analog Inputs

Number of Channels	16	
A/D Resolution	12 bits	
A/D Conversion Time	80ns	
Number of ADC's	1 (8 channels are multiplexed on-chip to form a bank)	
Number of S/H units	2 (each bank has one sample and hold unit)	
Reference Voltages	ADCINA6, ADCINB6	2.5V
	ADCINA7, ADCINB7	1.25V

2.2.1 AC General Inputs

Definition	12 off 0-3V analog inputs with low pass filter capacitors ADCINA0-5 ADCINB0-5
Input Voltage Range	0-3V maximum
Dynamic Response	Cut-off frequency >150kHz
PCB Connections	ADCINA0-5 on 26-way IDC header (**X8**) ADCINB0-5 on 26-way IDC header (**X7**)

2.3 Digital I/O

Definition	8 bits total Digital I/O Expansion Port 0x07 addressable through the SPI Interface
Digital high input voltage threshold	4.0V
Digital low input voltage threshold	1.0V
Interrupt Capable	Yes, Common Digital Interrupt Input to CAP3 on the DSP
Digital I/O rated at	Source 3mA per bit, ABSOLUTE MAXIMUM Sink 8mA per bit, ABSOLUTE MAXIMUM
PCB Connection	DIGIOA4-7 – 16-way IDC header (**X7**) DIGIOA0-3 – 16-way IDC header (**X8**)

2.4 Digital Inputs

2.4.1 Interrupt Capable Digital Inputs

Definition	7 bits total 2 off PDPINT* Gate Driver Interrupt Inputs (PDPINTA*, PDPINTB*) 2 off TTL-level External Interrupt Inputs (zener clamped) (XINT2, XINT3) 1 off TTL-level External Interrupt Input (XINT1) 2 off TTL-level Capture Port Inputs (CAP1, CAP6) Note: Digital I/O Expansion Port 0x07 can be configured to be interrupt driven providing 8 additional indirect interrupt driven inputs
Digital high input voltage threshold	3.85V
Digital low input voltage threshold	1.65V
Digital I/O rated at	±24mA per bit, ABSOLUTE MAXIMUM
PCB Connection	PDPINTA* (GATE_FAULTA*) – 26-way IDC header (**X6**) PDPINTB* (GATE_FAULTB*) – 26-way IDC header (**X5**) CAP1 (ZX), XINT1 (INT1), CAP6 (SPI_INT*) – 26-way IDC header (**X9**) XINT2 (INT2), XINT3 (INT3) – 14-way IDC header (**X2**)

2.5 Digital Outputs

2.5.1 Open Collector Digital Outputs

Definition	8 bits total of Open Collector Digital Outputs (can be referenced to +5V or +12V) Digital Output Expansion Port 0x07 addressable through the SPI Interface
PCB Connection	DIGIOB0-7 – 14-way IDC header (**X2**)

2.5.2 3.3V-TTL Level Digital Outputs

Definition	GPIOF11, F14
Digital outputs rated at	±4mA per bit, ABSOLUTE MAXIMUM
PCB Connection	GPIOF11 & F14 – 10-way IDC header (**X10**)

2.6 PWM Gate Drive Interface – EVA

Definition	1 off 8 PWM Outputs within Event Manager A
PWM Outputs per Event Manager	Event manager has 8 PWM outputs consisting of – 3 independent complementary pairs (6 outputs) with programmable deadband generation 2 gate drive outputs generated from two independent outputs, for which deadband compensation must be implemented in software
Gate Fault Interrupt	PDPINTA*, which when unmasked and activated, immediately disables the PWM outputs. Response time is ~12nsec after fault detection The PWM signals are placed into a high impedance state and have on-card pull-down resistors
Gate Reset	Normally Low Gate Reset Signal
Output Voltage	0-5V
PCB Connections	26-way IDC header (**X6**)

2.7 PWM Gate Drive Interface – EVB

Definition	1 off 8 PWM Outputs within Event Manager B
PWM Outputs per Event Manager	Event manager has 8 PWM outputs consisting of – 3 independent complementary pairs (6 outputs) with programmable deadband generation 2 gate drive outputs generated from two independent outputs, for which deadband compensation must be implemented in software
Gate Fault Interrupt	PDPINTB*, which when unmasked and activated, immediately disables the PWM outputs. Response time is ~12nsec after fault detection The PWM signals are placed into a high impedance state and have on-card pull-down resistors
Gate Reset	Normally Low Gate Reset Signal
Output Voltage	0-5V
PCB Connections	26-way IDC header (**X5**)

2.8 Communications Interface

Definition	The TMS320F22810 has two off serial communications interface ports (SCIA and SCIB) and two off serial peripheral interfaces (SPI and McBSP)
Configuration	SCIA is operated as a 3.3V-TTL level serial port SCIB is configured as an isolated USB serial port The SPI interface is available at both 3.3V and 5V-TTL levels with separate chip selects

2.8.1 Serial Peripheral Interface – SPI

Definition	Four-pin serial peripheral interface (SPI) module. It is a high speed, synchronous serial I/O port that allows a serial bit stream of programmed length (one to sixteen bits) to be shifted into and out of the device at a programmable bit-transfer rate **DEFAULT MODE:** Configured as SPI Mode
Compatibility	3 wire SPI mode (with independent chip selects) Available as non-buffered, non-isolated 3.3V-TTL Level signals on **X10** Available as non-buffered, non-isolated 5V-TTL Level signals on **X9**
PCB Connection	10-way IDC connector (**X10**) Also available on 26-way IDC header (**X9**)

2.8.2 Serial Communication Interface – SCIA – TTL Level

Definition	Two-wire asynchronous serial port (UART) that supports a 16-level, receive and transmit FIFO for reducing servicing overhead. The receiver and transmitter are double buffered with separate enable and interrupt bits **DEFAULT MODE:** 3.3V-TTL level serial connection, providing two pin serial communications for interface to an off-card 3.3V-TTL level to RS-232 translation card. This is necessary for interfacing to a standard PC serial port
Isolation	None
Communications Port	SCIA
PCB Connections	4-way pin strip header with VDD and GND connections (**X1**)

2.8.3 Serial Communication Interface – SCIB

Definition	Two-wire asynchronous serial port (UART) that supports a 16-level, receive and transmit FIFO for reducing servicing overhead. The receiver and transmitter are double buffered with separate enable and interrupt bits
Communications Port	SCIB
Isolation	HCPL-2211 1000V isolation (Please consult the datasheet for this component for full isolation information)
USB Interface	USB PC Drivers available from Future Technology Devices International Limited website http://www.ftdichip.com Install drivers onto the PC, attach the CPT-R09 board to the USB connection and the USB device should be automatically detected and installed Refer to *Windows_XP_Installation_Guide.pdf* for full installation instructions
Shield termination	Linkable to USB ground (**X11**)
PCB Connections	5 pin MOLEX connector (**X4**) or USB Type B standard connector (**X3**)

2.9 JTAG

Definition	DSP interface connection, which enables the TMS320F2810 to interface to an ICE to provide a real-time debugging environment
Compatibility	Compatible with IEEE 1149.1 standard for scan-based emulation
PCB Connection	14-way IDC connector (**X12**)

2.10 Software

Standard Support Software	Monitor Program, standard library source code, sample programs Texas Instruments: Code Composer Studio V3 and above

2.11 General

Physical Dimensions	L: 150mm
	W: 115mm
	H: 50mm approx.
Mounting Arrangement	6 off 3.5 mm holes – please consult the mechanical layout diagram in the appendix for full details
Environmental	-20 – 75°C ambient operating temperature 5% - 95% non condensing humidity

2.12 Power Supply

Input Voltage Nominal	12V DC
Input Voltage Range	8VDC – 20V DC
Standalone Input Current	**TBD** (depending on the active sections within the DSP)
Max Input Power	Approx. **TBD ~8W**
Supplies Generated on-card	+12V (+12V) used for generating all on-card regulated power supplies
	+12R (+12V) Filtered Power Supply (available on connector **X9**)
	+5V_DIG (+5V) Digital Supply (filtered +5V_DIG_FLT and +5V_DIG_FLTB)
	VDD / VCC (+3.3V) Digital
	AVDD (+3.3V) Analog DSP Supply
	VDDCORE (+1.9V) DSP Core
	AVCCCORE (+1.9V) Analog Section DSP Core
	+2.5V Analog Reference (2.5V_OC off-card filtered reference)
USB Power Supply	Supply is generated from the USB Cable, **X3**
Input Power Connector	4 pin plug-in PCB Mounting Terminal Block with 2 off +12V and 2 off GND connections, (**X13**)

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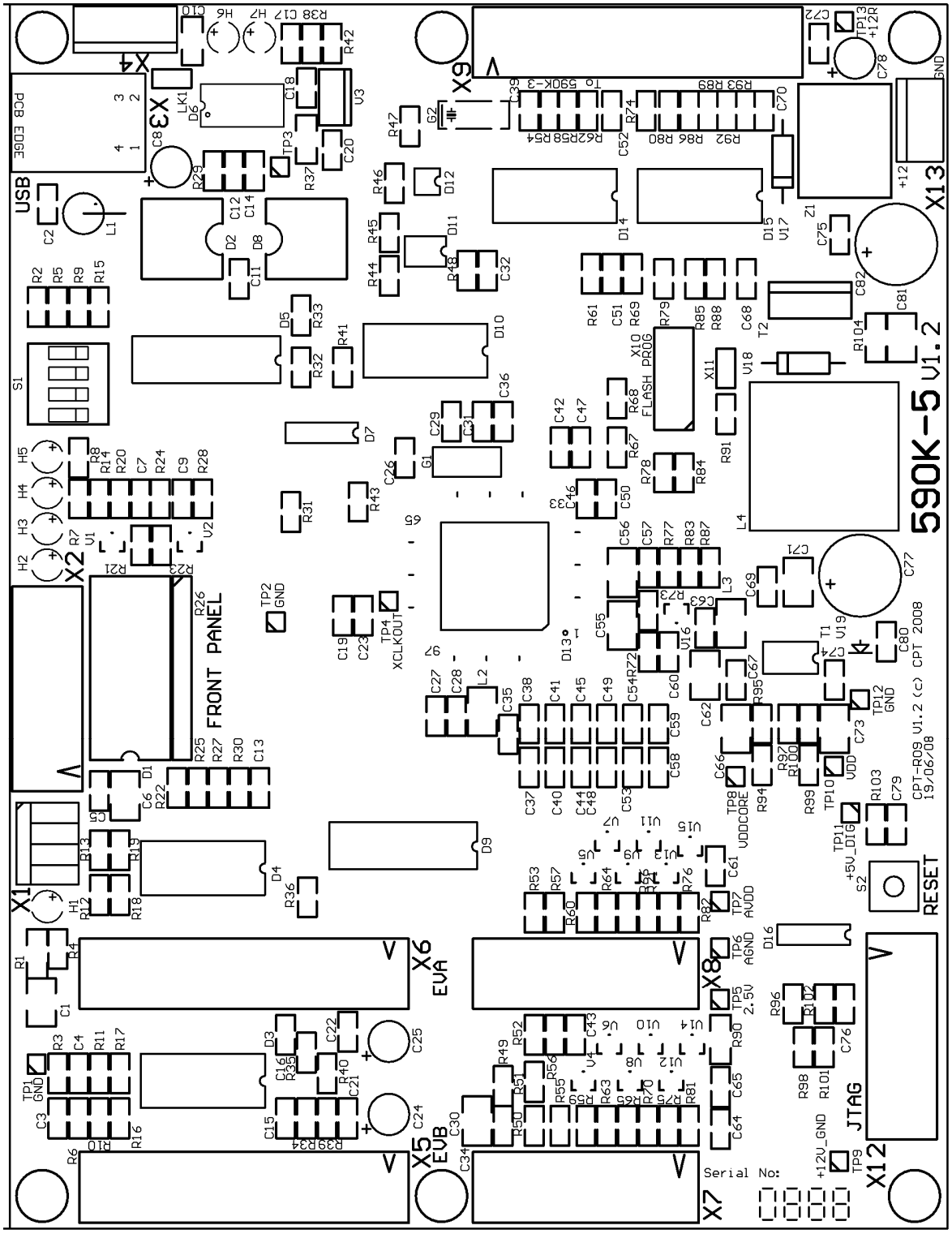
Appendices

Appendix A Component Layout

Top Layer



Appendix B Mechanical Layout